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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/784,151	02/16/2001	Yusuke Kawasaki	108066-00030	2129

7590 05/13/2005

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EXAMINER	
DAVIS, ZACHARY A	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/784,151	KAWASAKI ET AL.	
	Examiner	Art Unit	
	Zachary A. Davis	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. An amendment was received on 07 March 2005 in response to a Notice of Non-Compliant Amendment. Claims 1, 3, 4, 6, 8-11, and 13-17 have been amended. No claims have been added or canceled. Claims 1-17 are currently pending in the present application.

Response to Arguments

2. Applicant's arguments filed 29 November 2004 have been fully considered but they are not persuasive.

Regarding the rejection of Claims 1-3, 5-8, 10-13, and 15-17 under 35 U.S.C. 103(a) as unpatentable over Yishay et al, US Patent 5704039, in view of Akiyama et al, US Patent 5784464, and specifically in reference to Claim 1, Applicant argues that Yishay does not disclose an internal circuit that includes a CPU connected to a debug interface circuit through a debug bus and a peripheral circuit connected to the CPU through an internal bus separated from the debug bus. However, the Examiner believes that Yishay does indeed disclose a circuit that includes a CPU (Figure 1, CPU 12) connected to a debug interface circuit through a debug bus (Figure 1, CPU security buffer 13 and bus 24) and a peripheral circuit (Figure 1, Circuits 14, 16, 18, and 20) connected to the CPU through an internal bus separated from the debug bus (Figure 1, Bus 36).

Regarding the rejection of Claims 4, 9, and 14 under 35 U.S.C. 103(a), in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Specifically, Applicant argues that Matsumura does not disclose or suggest the authentication circuit waiting to enable operation following an authentication. However, the Examiner believes that Matsumura clearly discloses waiting to return the processing result of a command after the performance of the command (column 3, line 66-column 4, line 5); the Examiner further believes that this teaching, taken in combination with Yishay and Akiyama's method that includes the performance of an authentication, would render obvious the step of waiting to return the processing result of an authentication operation after the performance of the authentication, where the authentication is the command.

Further regarding Claims 4, 9, and 14, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation was as stated in the previous Office action, namely to prevent unauthorized use by preventing processing results or commands

from being determined by measuring processing time, as taught by Matsumura, column 2, lines 23-41.

Therefore, for the reasons detailed above, the Examiner maintains the rejections as set forth below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-8, 10-13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yishay et al, US Patent 5704039, in view of Akiyama et al, US Patent 5784464.

In reference to Claim 1, Yishay discloses an IC including an internal circuit and a debug interface circuit (column 6, lines 56-62). Yishay further discloses an authentication circuit that authenticates based on a signal received from a debug terminal in order to enable operation of the debug interface circuit (column 6, lines 6-11). Yishay also discloses a circuit that includes a CPU (Figure 1, CPU 12) connected to a debug interface circuit through a debug bus (Figure 1, CPU security buffer 13 and bus 24) and a peripheral circuit (Figure 1, Circuits 14, 16, 18, and 20) connected to the CPU through an internal bus separated from the debug bus (Figure 1, Bus 36).

However, Yishay does not explicitly disclose transmitting a transmission key outside of the device, nor does Yishay explicitly disclose using the transmission key with the received signal to authenticate.

Akiyama discloses a method for authenticating a client in which a transmission key is sent outside the authenticating device (column 11, lines 62-67) and authentication is performed by comparing the transmission key and a signal received from outside the authenticating device (column 12, lines 10-29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Yishay by including the authentication method as disclosed by Akiyama, in order to increase the security of the device by making it impossible for a third party to use the authentication and identification data (see Akiyama, column 2, lines 10-16).

In reference to Claim 2, Yishay further discloses a reset signal and enabling operation of the debug interface (column 4, lines 49-52).

In reference to Claims 3 and 5, Akiyama further discloses that an authentication key is generated by encrypting the transmission key, which is a random number, with a predetermined key (column 12, lines 3-6 and 13-20). Akiyama also discloses that the received signal is compared with the authentication key (column 12, lines 20-23).

Claims 6-8 and 10 are directed to a device including an IC as disclosed in claims 1-3 and 5, respectively, and are rejected by a similar rationale.

Similarly, Claims 11-13 and 15 are directed to a method corresponding substantially to the IC of claims 1-3 and 5, respectively, and are rejected by a similar rationale.

In reference to Claim 16, Akiyama further discloses receiving the transmission key and encrypting the transmission key with a predetermined key (column 12, lines 3-6), and transmitting the encrypted key using a client (column 12, lines 6-9).

In reference to Claim 17, Yishay discloses a debugger for an IC that includes an internal circuit, a debug interface circuit (column 6, lines 56-61), and an authentication circuit (column 6, lines 6-11). Yishay further discloses a debug unit and discrimination device (column 6, lines 59-61). Yishay additionally discloses a circuit that includes a CPU (Figure 1, CPU 12) connected to a debug interface circuit through a debug bus (Figure 1, CPU security buffer 13 and bus 24) and a peripheral circuit (Figure 1, Circuits 14, 16, 18, and 20) connected to the CPU through an internal bus separated from the debug bus (Figure 1, Bus 36). However, Yishay does not disclose that the discrimination device receives a transmission key from the authentication circuit, encrypts the transmission key with a predetermined key, and transmits the encrypted key to the authentication circuit.

Akiyama discloses a method for authenticating a client in which a transmission key is received and encrypted with a predetermined key (column 12, lines 3-6), and further transmitted to an authentication device (column 12, lines 6-9). Therefore, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Yishay by including the authentication method as disclosed by Akiyama, in order to increase the security of the device by making it impossible for a third party to use the authentication and identification data (see Akiyama, column 2, lines 10-16).

5. Claims 4, 9, and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Yishay in view of Akiyama as applied to claims 1, 6, and 11 above, and further in view of Matsumura et al, US Patent 4908038.

Yishay as modified above discloses everything as applied to Claims 1, 6, and 11 above. However, neither Yishay nor Akiyama teach waiting a specified amount of time before enabling the operation of the debug interface. Matsumura discloses a high security IC card, which includes a timer circuit that measures a pre-determined elapsed time before returning a processing result (column 3, line 66-column 4, line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the IC, device, and method as taught by Yishay as modified above, in order to prevent unauthorized use by preventing the processing results or command from being determined by measuring the processing time (see Matsumura, column 2, lines 23-41).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zachary A. Davis whose telephone number is (571) 272-3870. The examiner can normally be reached on weekdays 8:30-6:00, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571) 272-3868. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Caldwell

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ANDREW CALDWELL
SUPERVISORY PATENT EXAMINER